

Intel® C600 Series Chipset

Thermal/Mechanical Design Guidelines

March 2012



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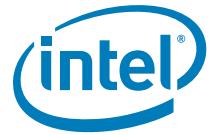


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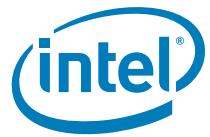
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Revision History

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1 Introduction

As the complexity of computer systems increases, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Typical methods to improve heat dissipation include selective use of ducting, and/or passive heatsinks.

The goals of this document are to:

- Outline the thermal and mechanical operating limits and specifications for the Intel® C600 Series Chipset.
- Describe reference thermal solutions that meet the specifications of the Intel® C600 Series Chipset

Properly designed thermal solutions provide adequate cooling to maintain the Intel® C600 Series Chipset case temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the case to local-ambient thermal resistance. By maintaining the Intel® C600 Series Chipset case temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the component. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

The simplest and most cost effective method to improve the inherent system cooling characteristics is through careful chassis design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

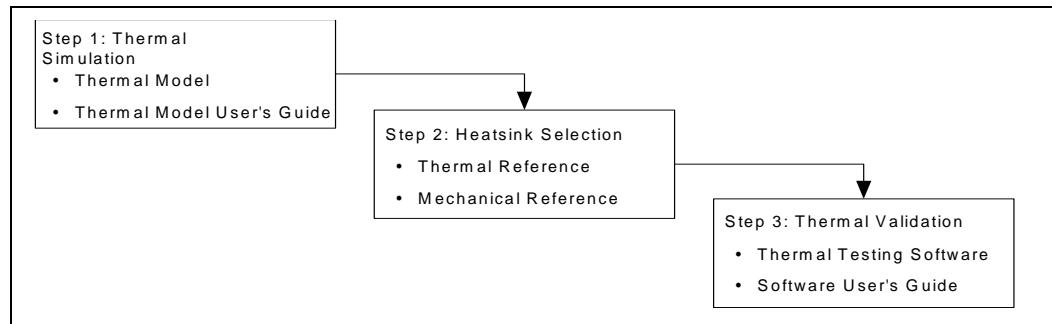
This document addresses thermal design and specifications for the Intel® C600 Series Chipset component only. For thermal design information on other chipset components, refer to the respective component TMSDG.

Note: Unless otherwise specified, the term "PCH" refers to the Intel® C600 Series Chipset.

1.1 Design Flow

To develop a reliable, cost-effective thermal solution, several tools have been provided to the system designer. [Figure 1-1](#) illustrates the design process implicit to this document and the tools appropriate for each step.

Figure 1-1. Thermal Design Process





1.2 Definition of Terms

BLT	Bond Line Thickness. Final settled thickness of the thermal interface material after installation of heatsink.
CTE	Coefficient of Thermal Expansion. The relative rate a material expands during a thermal event.
FC-BGA	Flip Chip Ball Grid Array. A package type defined by a plastic substrate where a die is mounted using an underfill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. Note that the device arrives at the customer with solder balls attached.
PCH	Platform Controller Hub. It is connected to the CPU via DMI2 and PCIe* Gen3, providing enhanced storage capabilities.
T _{case_max}	Die temperature allowed. This temperature is measured at the geometric center of the top of the die.
TDP	Thermal design power. Thermal solutions should be designed to dissipate this target power level. TDP is not the maximum power that the PCH can dissipate.

1.3 Reference Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents:

Title	Document #	Location
Intel® C600 Series Chipset Datasheet	326514-001	www.intel.com
Intel® C600 Series Chipset Specification Update	326515-001	www.intel.com
Various system thermal design suggestions (http://www.formfactors.org)		

Note: Unless otherwise specified, these documents are available through your Intel field sales representative. Some documents may not be available at this time.

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2 Packaging Technology

2.1 PCH Package

The Intel® C600 Series Chipset component uses a 27.0 mm square, 8-layer flip chip ball grid array (FC-BGA) package (see [Figure 2-1](#), [Figure 2-2](#) and [Figure 2-3](#)).

Figure 2-1. PCH Package Dimensions (Top View)

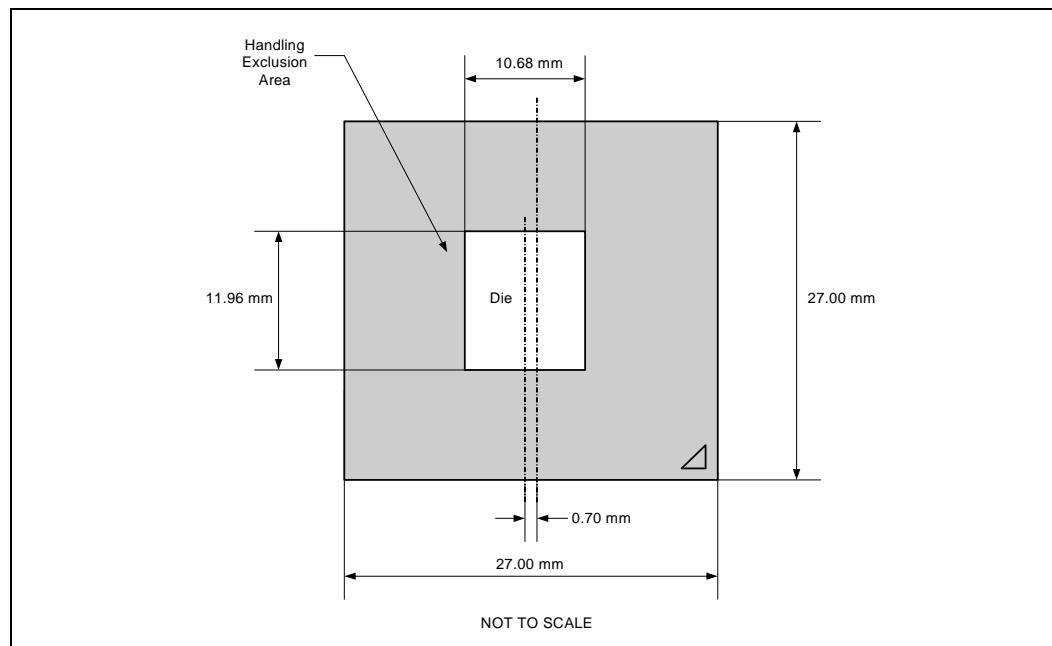


Figure 2-2. PCH Package Dimensions (Side View)

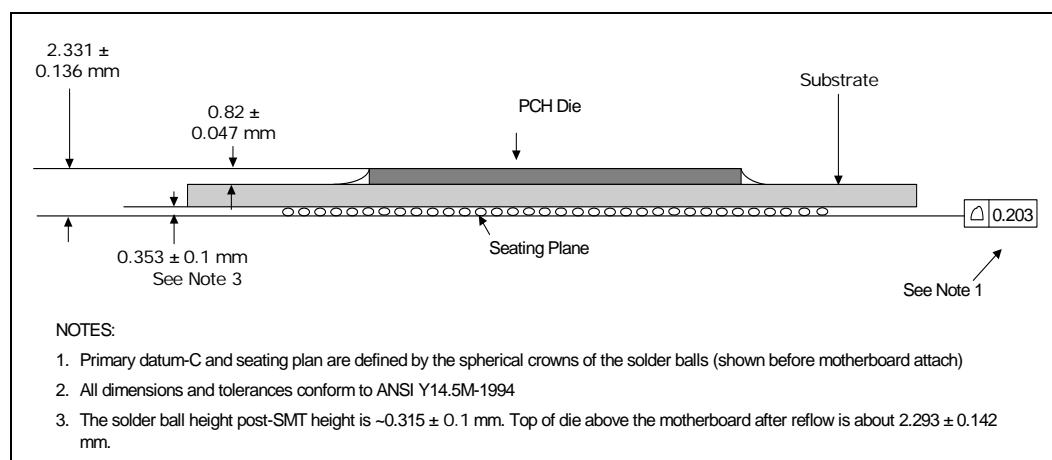
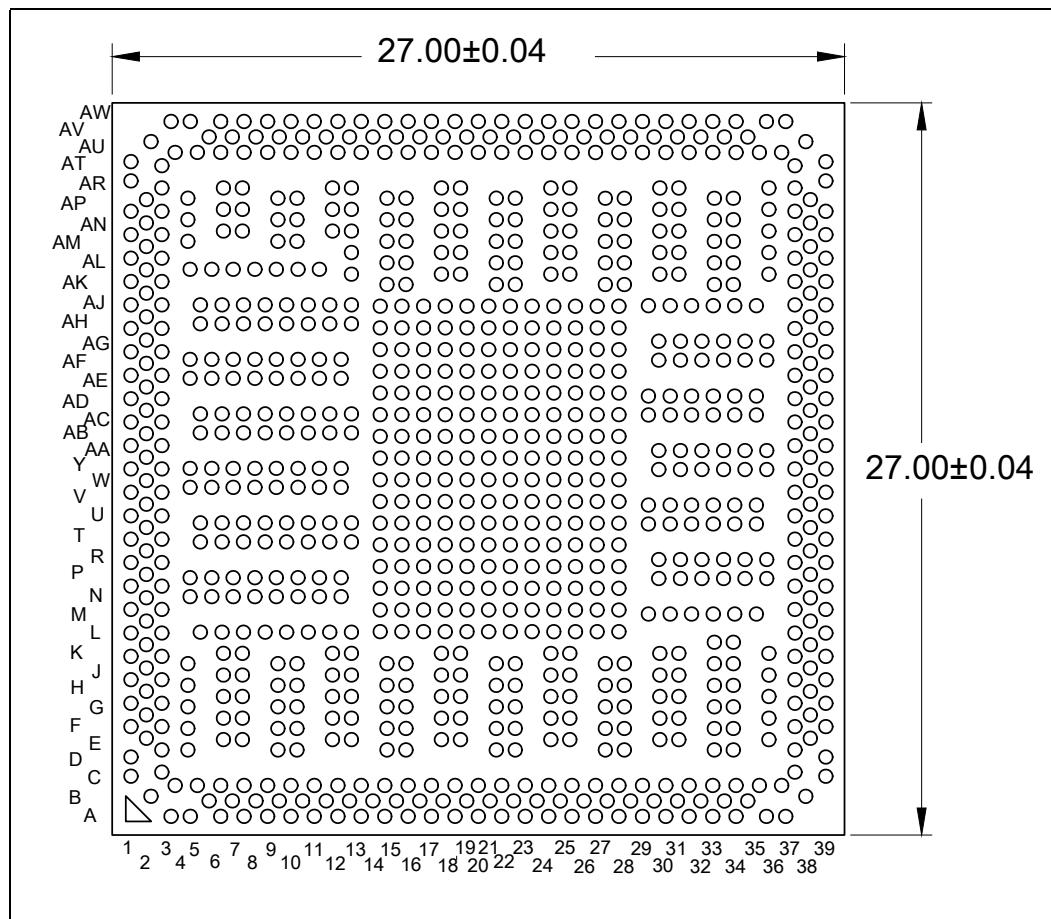


Figure 2-3. PCH Package Dimensions (Bottom View)



Notes:

1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M-1994.

2.2

PCB Pad Recommendations

Intel recommends customers implement the board pad sizes and types shown in [Table](#) and [Figure 2-4](#) for PCH printed circuit board (PCB) designs. These recommendations allow for trace breakout in a typical 8 layer board design. In addition the corner pads design has been optimized for mechanical strength and protection to inner critical to function interconnects. The PCH PCB CAD symbol has the recommended pad sizes and types implemented. See [Section 1.3, “Reference Documents”](#) for the document number of the PCH symbol.

2.2.1

Pad Type Recommendations

In the PCH footprint, Intel defines two pad types based on how the pad is constructed. A metal defined (MD) pad is one where a copper pad is individually etched into the PCB with a minimum width trace exiting it. The solder mask defined (SMD) pad is typically a pad in a flood plane where the solder mask opening defines the pad size for soldering to the component.

In thermal cycling a MD pad is more robust than a SMD pad type. The solder mask that defines the SMD pad can create a sharp edge on the solder joint as the solder ball / paste conforms to the window created by the solder mask.

The solder joints under the die (die shadow) can experience increased stress due to a coefficient of thermal expansion (CTE) mismatch between the package and board. The size of the die tends to influence the localized CTE of the package substrate driving higher stresses on the solder joints under the die shadow. For this reason the recommended pad type in this region is MD.

For certain failure modes the MD pad may not be as robust in shock & vibration (S&V). During S&V, the predominant failure mode for a MD pad in the corner of the BGA layout is pad crater and solder joint cracking. A corner MD pad can be designed to absorb more dynamic energy by having a wide trace exiting the pad if other escape routing constraints allow. This trace should be 10 mils minimum but should not exceed the pad diameter and exit the pad at a 45 degree angle (parallel to the diagonal of the package). During board flexure that results from shock & vibration a SMD pad is less susceptible to a crack initiating due to the larger surface area. See [Chapter 7](#) for additional details on wide traces and additional guidance on design recommendations for solder joint reliability.

Figure 2-4. Pad Size and Shape Recommendations (looking at PCB land)

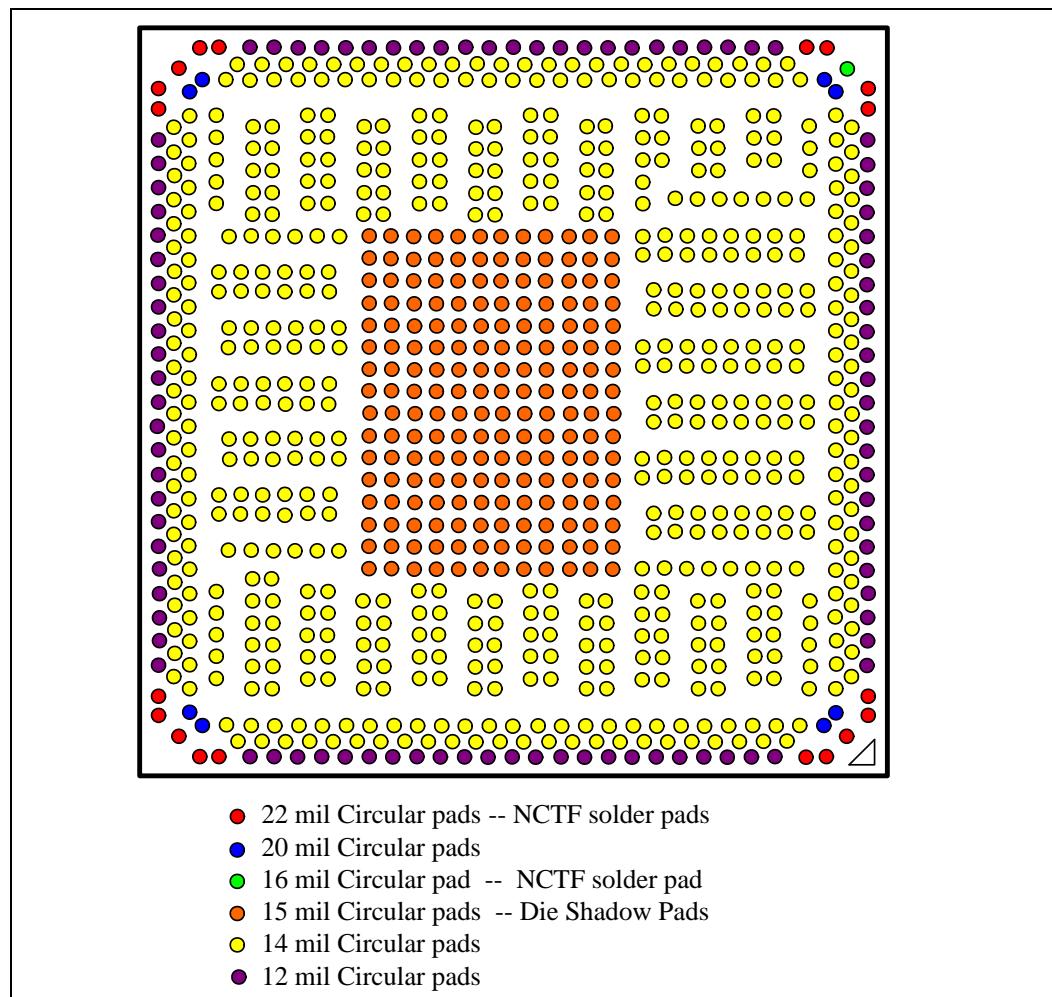


Table 1. Pad Size / Geometry and Type Recommendations

Pad Size (Diameter)/Shape	Type	Solder Resist Opening (SRO)	Location	Comment
22 mil Circular	Solder Mask Defined with wide trace	16 mil	Corner of PCB layout (Red Pins)	Non Critical to Function Pads See note 1, 2
20 mil Circular	Solder Mask Defined	14 mil	Corner of PCB layout (Blue Pins)	N/A
16 mil Circular	Metal Defined with wide trace	N/A	Ball AV2 (Green Pin)	See Note 1, 2, 3
15 mil Circular	Metal Defined	N/A	Inner pads of PCB layout (Orange Pins)	See Note 4, 5
14 mil Circular	Metal Defined	N/A	Inner pads of PCB layout (Yellow Pins)	N/A
12 mil Circular	Metal Defined with wide trace	N/A	Perimeter of PCB layout (Purple Pins)	See Note 1

Notes:

1. wide traces should be 10 mil minimum width but not to exceed the pad diameter.
2. The wide trace exiting the pad 45 degree angle (parallel to the diagonal of the package).
3. Due to signal integrity requirements, this location will be designed as 16 mil diameter metal defined with width trace.
4. The pads in the die shadow area should be MD where possible.
5. The board solder mask registration tolerance must be $\pm 2.25\text{mil}$ for this pad size

2.2.2

Non-Critical to Function Solder Joints

Intel has defined selected solder joints of the PCH as non-critical to function (NCTF) when evaluating package solder joints post environmental testing. The PCH signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality. [Figure 2-4](#) identifies the NCTF solder joints of the PCH package.

Under typical loading conditions from the Intel® C600 Series Chipset thermal solution, the solder joints at the component corners may experience stresses that can create opens. These opens in the corners typically occur during shipping or thermal cycling stresses.

2.3

Package Mechanical Requirements

The Intel® C600 Series Chipset package has a bare die that is capable of sustaining a maximum static normal load of 15 lbf (67N). These mechanical load limits must not be exceeded during heatsink installation, mechanical stress testing, standard shipping conditions and/or any other use condition.

Note:

The heatsink attach solutions must not include continuous stress to the PCH package with the exception of a uniform load to maintain the heatsink-to-package thermal interface.

Note:

These specifications apply to uniform compressive loading in a direction perpendicular to the die top surface.

Note:

These specifications are based on limited testing for design characterization. Loading limits are for the package only.

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3 Thermal Specifications

3.1 Thermal Design Power (TDP)

Analysis indicates that real applications are unlikely to cause the PCH component to consume maximum power dissipation for sustained time periods. Therefore, in order to arrive at a more realistic power level for thermal design purposes, Intel characterizes power consumption based on known platform benchmark applications. The resulting power consumption is referred to as the Thermal Design Power (TDP). TDP is the peak power level to which the thermal solutions should be designed. TDP numbers assume standard ASPM power-management features use.

For TDP specifications, see [Table](#), [Table 3-2](#) and [Table 3-3](#) for the Intel® C600 Series Chipset. FC-BGA packages have poor heat transfer capability into the board and have minimal thermal capability without thermal solution. Intel recommends that system designers plan for a heatsink for most Intel® C600 Series Chipset configurations. A specific low-power minimal feature-use configuration has been defined for the -A SKU to support heatsink-less basic platform designs.

Table 3-1. Intel® C600 Series Chipset -A/B SKU Configurations Thermal Design Power

Configuration	Full-Feature/ Workstation Config	Server Config	Lite/Low Power Config	Notes
SCU SAS/SATA ports	4 (6G)	4 (6G)	Unused	
AHCI SATA 6G ports	2 (6G)	2 (6G)	Unused	
AHCI SATA 3G ports	4	4	2	
USB	14	6	6	
PCIe expansion ports	8 ¹	6	4	See Note 1
Manageability Engine	AMT	DCMI / NM	Ignition only	
1 GbE MAC	Enabled	Disabled	Disabled	
Legacy 32b PCI port	Routed/used	Unused ²	Unused ²	See Note 2
HD Audio	Routed/used	Unused	Unused	
TDP max (W)	7.8	6.7	5.4	See Note 3
Idle Power typ (W) (Max)	2.5 (3.6)	2.4 (3.5)	1.9 (2.9)	See Note 4

**Table 3-2. Intel® C600 Series Chipset -D/T SKU Configurations Thermal Design Power
(Sheet 1 of 2)**

Configuration	Full-Feature Config	Workstation Config	Server Config	Notes
SCU SAS/SATA ports	8 (6G)	8 (6G)	8 (6G)	
AHCI SATA 6G ports	2 (6G)	2 (6G)	2 (6G)	
AHCI SATA 3G ports	4	1	0	
USB	14	14	6	
PCIe expansion ports	8 ¹	6	6	
Manageability Engine	DCMI/NM	AMT	DCMI/NM	

**Table 3-2. Intel® C600 Series Chipset -D/T SKU Configurations Thermal Design Power (Sheet 2 of 2)**

1 GbE MAC	Enabled	Enabled	Disabled	See Note 1
Legacy 32b PCI port	Routed/used	Routed/used	Unused ²	See Note 2
HD Audio	Routed/used	Routed/used	Unused	
TDP max (W)	11.4	11.3	10.8	See Note 3
Idle Power typ (W) (Max)	3.9 (6.85)	3.9 (6.85)	3.9 (6.85)	See Note 4

Table 3-3. Intel® C600 Series Chipset -J SKU Configurations Thermal Design Power

Configuration	Full-Feature Config	Lite/Low Power Config		Notes
AHCI SATA 6G ports	2	Unused		
AHCI SATA 3G ports	4	2		
USB	14	6		
PCIe expansion ports	8 ¹	4		See Note 1
Manageability Engine	AMT	Ignition only		
1 GbE MAC	Enabled	Disabled		
Legacy 32b PCI port	Routed/used	Unused ²		See Note 2
HD Audio	Routed/used	Unused		
TDP max (W)	6.7	5.4		See Note 3
Idle Power typ (W) (Max)	2.5 (3.6)	1.9 (2.9)		See Note 4

Notes:

1. Use of 1 GbE MAC occupies 1 of available PCIe expansion ports.
2. PCI bus subtractive decode disabled, directed to PCIe expansion ports
3. TDP power (max) represents required thermal design solution capacity required to support 3-sigma manufacturing variance.
4. Idle power (typ) is representative average across volume distribution
5. Configurations are typical usages for the purposes of identifying best approximate TDP values. Intel does not quote power consumption on a per-port or per-feature basis.
6. These specifications are based on both pre-silicon estimates and simulations, as well as verified via post-Si correlation.

3.2 Case Temperature

To ensure proper operation and reliability of the Intel® C600 Series Chipset, the case temperature must be following the thermal profile as specified in [Table 3-4](#). System and/or component level thermal solutions are required to maintain these temperature specifications. Refer to [Chapter 5](#) for guidelines on accurately measuring package case temperatures.

Table 3-4. Intel® C600 Series Chipset Thermal Specification

Parameter	-A,-B	-D,-T	-J
Tcase_max	92.7 °C	92.7 °C	92.7 °C
Tcase_min	5 °C	5 °C	5 °C
Tcontrol	85 °C	85 °C	85 °C

**Notes:**

1. When Tsensor < Tcontrol, which means the component thermal sensor reading is less than Tcontrol, system fans can be under any condition.
2. When Tsensor >= Tcontrol, which means component thermal sensor reading is larger than Tcontrol. The fan speed must increase as necessary to try to maintain the Tsensor less than Tcontrol. In the case where maximum fan speed is reached and Tsensor cannot be maintained less than Tcontrol, the Tcase_max must still be maintained to be less than or equal.
3. Tcontrol value should be compared with the reading data from the digital thermal sensor embedded in package for system fan speed control.

Note:

The Intel® C600 Series Chipset silicon has an on die thermal sensor which is intended for usage in fan speed control and thermal management to allow optimal acoustic without introducing thermal risk. When evaluating the thermal requirements under lower power and fan speeds, make sure to use engineering judgment on the airflow requirements taking the thermal sensor and fan speed control capability into account. The thermal solution should be designed to have sufficient head room to cover TDP under maximum ambient and altitude conditions, however it is up to the thermal engineer to determine the quality, risk and cost regarding the acoustic solution.

3.3 Storage Specifications

Table 3-5 includes a list of the specifications for device storage in terms of maximum and minimum temperatures and relative humidity. These conditions should not be exceed in storage or transportation.

Table 3-5. Storage Conditions

Parameter	Description	Min	Max	Notes
T _{Absolute Storage}	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to for any length of time.	-55°C	125°C	1,2,3
T _{Sustained Storage}	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5°C	40°C	4,5
RH _{Sustained Storage}	The maximum device storage relative humidity for a sustained period of time.	60% @ 24 °C		5,6
TIME _{Sustained Storage}	A prolonged or extended period of time; typically associated with customer shelf life.	0 month	6 month	6

Notes:

1. Refer to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperature are based on data collected. Exceptions for surface mount reflow are specified in by applicable JEDEC standard and MAS document. Non-adherence may affect component reliability.
3. Tabsolute storage applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags or desiccant.
4. Intel® branded board products are certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40°C to 70°C & Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28°C) Post board attach storage temperature limits are not specified for non-Intel® branded boards.
5. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
6. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by Tsustained and customer shelf life in applicable Intel box and bags.

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4 Thermal Simulation

Intel provides thermal simulation models of the Intel® C600 Series Chipset and associated users' guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated, system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool FLOTHERM* (version 8.2 or higher) by Mentor Graphics, Inc. Contact your Intel field sales representative to order the thermal models and users' guides.

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Thermal Simulation



5 Thermal Methodology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the PCH die temperatures. [Section 5.1](#) provides guidelines on how to accurately measure the PCH die temperatures. The flowchart in [Figure 5-1](#) offers useful guidelines for thermal performance and evaluation.

5.1 Die Temperature Measurements

To ensure functionality and reliability, the T_{case} of the PCH must be maintained at or between the maximum/minimum operating range of the temperature specification as noted in [Table 3-4](#). The surface temperature at the geometric center of the die corresponds to T_{case} . Measuring T_{case} requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, and/or contact between the thermocouple cement and the heatsink base (if a heatsink is used). For maximum measurement accuracy, only the 0° thermocouple attach approach is recommended.

5.1.1 Zero Degree Angle Attach Methodology

1. Mill a 3.3 mm (0.13 in.) diameter and 1.5 mm (0.06 in.) deep hole centered (with 0.7mm offset to left side refer to [Figure 5-2](#)) on the bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot from the centered hole to one edge of the heatsink. The slot should be parallel to the heatsink fins (see [Figure 5-2](#)).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, ensure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see [Figure 5-3](#)).
6. Attach heatsink assembly to the PCH and route thermocouple wires out through the milled slot.

Figure 5-1. Thermal Solution Decision Flowchart

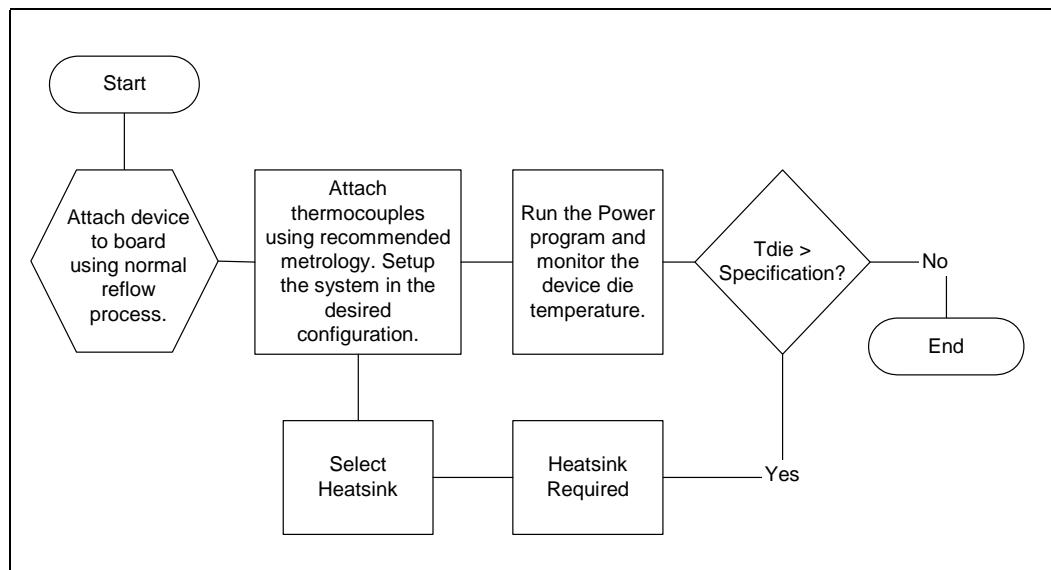
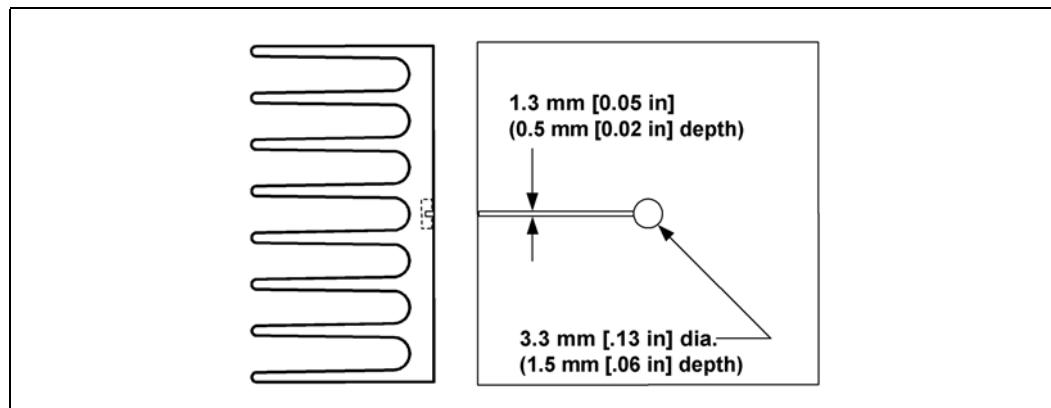
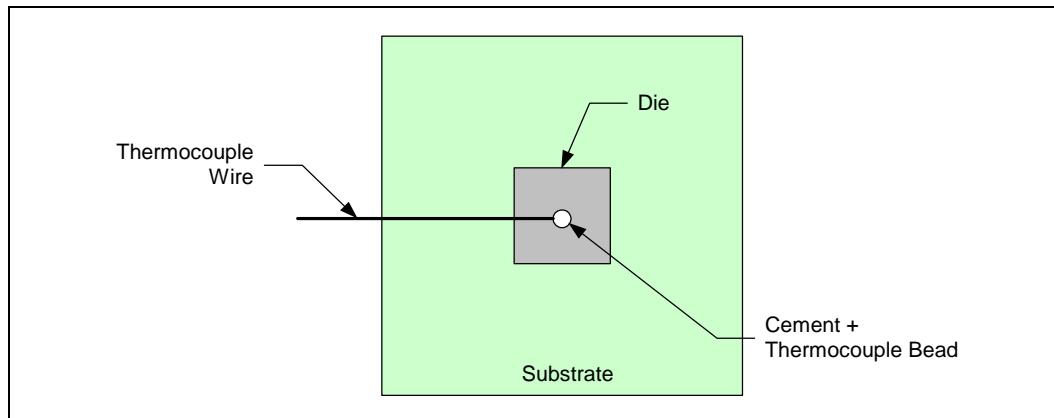


Figure 5-2. Zero Degree Angle Attach Heatsink Modifications



Note: Not to scale.

Figure 5-3. Zero Degree Angle Attach Methodology (Top View)

Note: Not to scale.

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6

Reference Thermal Solution

Intel has developed a reference thermal solutions to meet the cooling needs of the Intel® C600 Series Chipset under operating environments and specifications defined in this document. This section describes the overall requirements for the torsional clip heatsink reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need attached thermal solutions depending on your specific system local-ambient operating conditions.

6.1

Operating Environment

The reference thermal solution was designed assuming: For Intel® C600 Series Chipset -A/B, under the high fan speed condition, a maximum local-ambient temperature of 63°C and the minimum recommended airflow velocity through the cross-section of the heatsink fins is 1.2m/s; under the acoustic fan speed condition, a maximum local-ambient temperature of 50°C and the minimum recommended airflow velocity through the cross-section of the heatsink fins is 0.5m/s. For Intel® C600 Series Chipset -D/T, under the high fan speed condition, a maximum local-ambient temperature of 46°C and the minimum recommended airflow velocity through the cross-section of the heatsink fins is 1.1 m/s; under the acoustic fan speed condition, a maximum local-ambient temperature of 50°C and the minimum recommended airflow velocity through the cross-section of the heatsink fins is 0.5 m/s.

The approaching airflow temperature is assumed to be equal to the local-ambient temperature. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate. These local-ambient conditions are based on a 35°C (under high fan speed condition) / 25°C (under acoustic fan speed condition) external-ambient temperature at 1500m altitude. (External-ambient refers to the environment external to the system.)

Note:

The heatsink was designed considering all the boundary conditions in [Table 6-1](#) but only the worst case would have been used to design the heatsink.

Table 6-1. Intel® C600 Series Chipset Operating Conditions

	-A/-B		-D/-T	
	Acoustic	High Speed	Acoustic	High Speed
Velocity (m/sec)	0.5	1.2	0.5	1.1
Altitude (m)	1500	1500	1500	1500
Tsystem_ambient (°C)	25	35	25	35
Trise (°C)	25	28	25	11
TIA (°C)	50	63	50	46

6.2

Heatsink Performance

[Figure 6-1](#) depicts the *simulated* thermal performance of the reference thermal solution versus approach air velocity. Since this data was measured at sea level, a correction factor would be required to estimate thermal performance at other altitudes. [Table 6-2](#) shows the alpha, beta and gamma value.

The following equation can be used to correct any altitude:

$$\theta_{ca} = \alpha + \beta \times Q_{alt}^{-\gamma} \left(\frac{\rho_{alt}}{\rho_0} \right)^{-\gamma}$$

α , β and γ can be obtained from [Figure 6-1](#).

Q - "velocity through heatsink fin area (m/s)". Velocity is the value on X axis of [Figure 6-1](#).

ρ_{alt} - Air density at given altitude.

ρ_0 - Air density at sea level.

Figure 6-1. Torsional Clip Heatsink Measured Thermal Performance Versus Approach Velocity

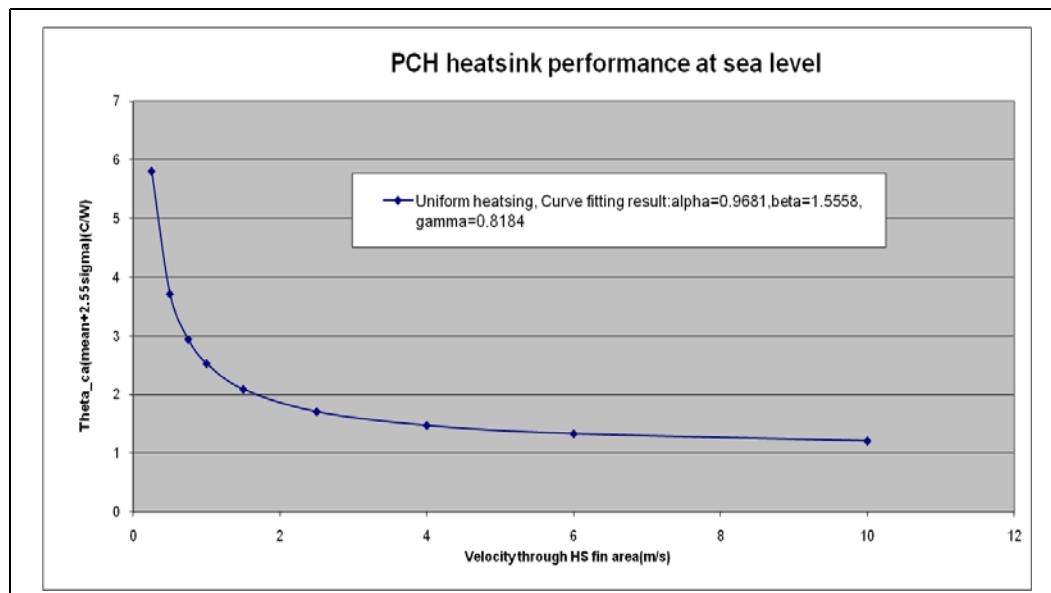


Table 6-2. Alpha, Beta and Gamma Values

	Alpha	Beta	Gamma
Value	0.9681	1.5558	0.8184

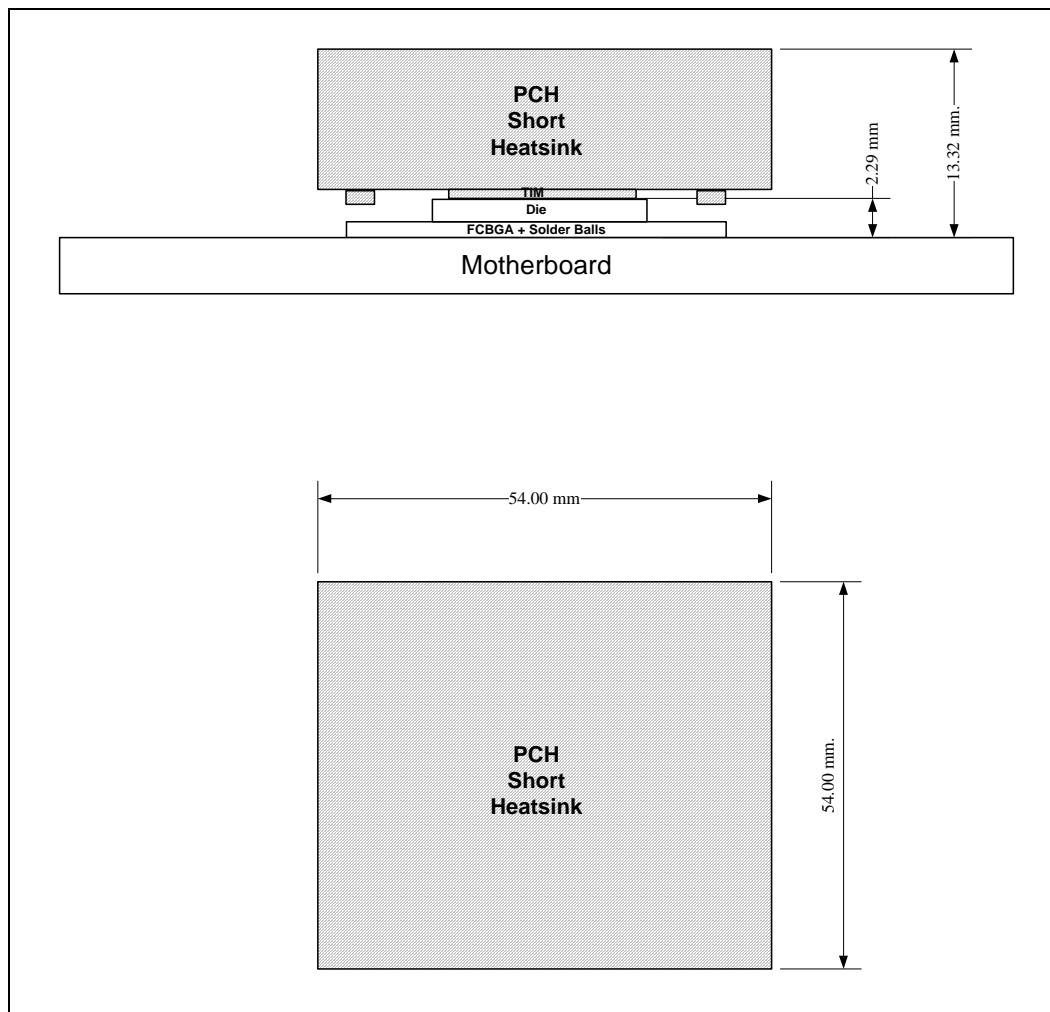
6.3

Mechanical Design Envelope

While each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the Intel® C600 Series Chipset thermal solution are shown in [Figure 6-2](#).

When using heatsinks that extend beyond the PCH reference heatsink envelope shown in [Figure 6-2](#), any motherboard components placed between the heatsink and motherboard cannot exceed height restriction under base area in corresponding direction.

Figure 6-2. Torsional Clip Heatsink Volumetric Envelope for the PCH



6.4 Board-level Components Keepout Dimensions

The location of hole patterns and keepout zones for the reference thermal solution are shown in [Figure 6-3](#) and [Figure 6-4](#).

6.5 Torsional Clip Heatsink Thermal Solution Assembly

The reference thermal solution for the PCH is a passive extruded heatsink with thermal interface. It is attached using a clip with each end hooked through an anchor soldered to the board. [Figure 6-5](#) shows the reference thermal solution assembly and associated components.

Full mechanical drawings of the thermal solution assembly and the heatsink clip are provided in [Appendix B](#). [Appendix A](#) contains vendor information for thermal solution assembly.

Figure 6-3. Torsional Clip Heatsink Board Component Keepout

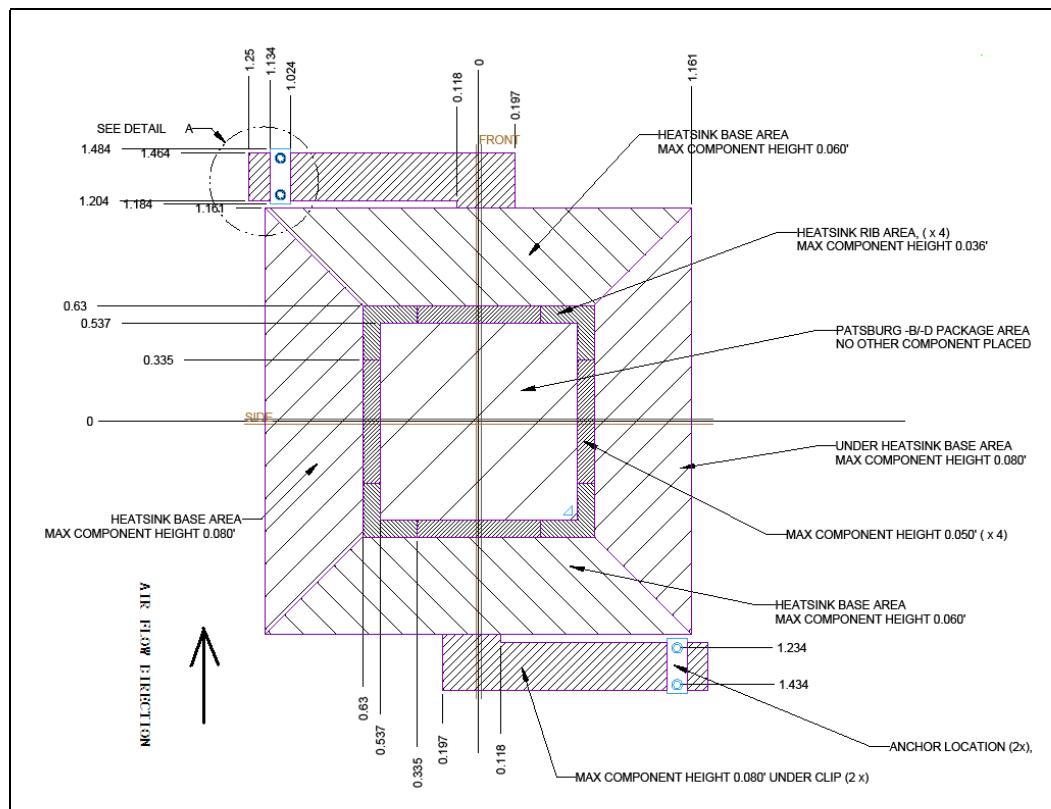
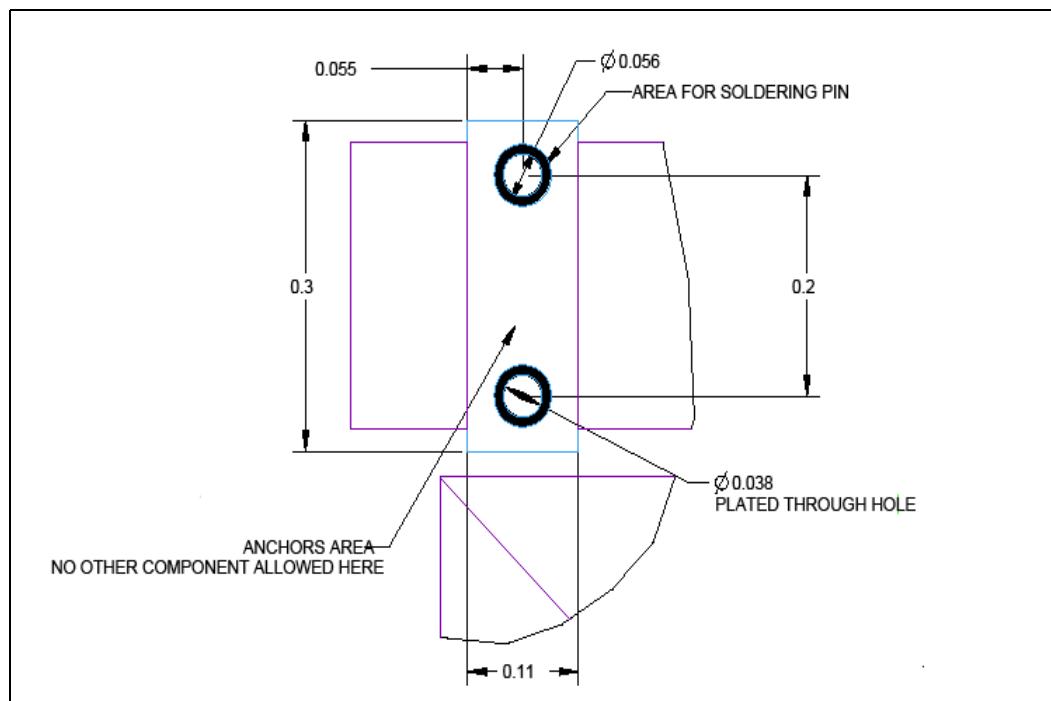


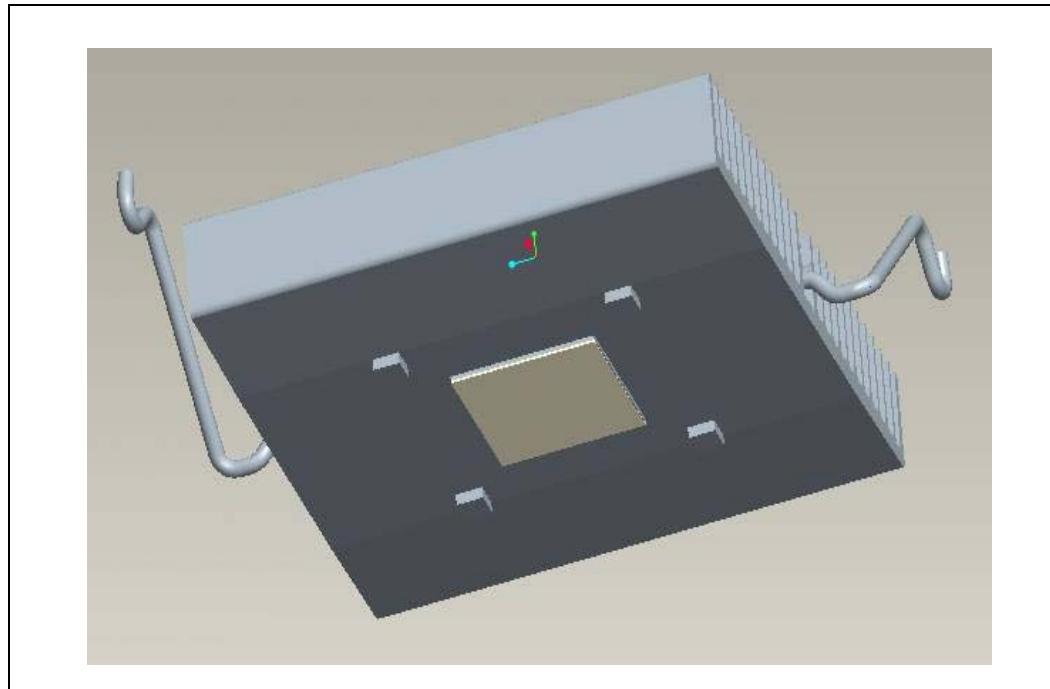
Figure 6-4. Retention Mechanism Component Keepout Zones



6.5.1 Heatsink Orientation

Since this solution is based on a unidirectional heatsink, mean airflow direction must be aligned with the direction of the heatsink fins.

Figure 6-5. Torsional Clip Heatsink Assembly



6.5.2 Extruded Heatsink Profiles

The reference thermal solution uses an extruded heatsink for cooling the PCH. [Figure 6-6](#) shows the heatsink profile. Other heatsinks with similar dimensions and increased thermal performance may be available. Full mechanical drawing of this heatsink is provided in [Appendix B](#).

6.5.3 Mechanical Interface Material

There is no mechanical interface material associated with this reference solution.

6.5.4 Thermal Interface Material

A thermal interface material (TIM) provides improved conductivity between the Die surface and heat sink. The reference thermal solution uses Honeywell PCM45 F*, 0.25 mm (0.010 in.) thick, 15 mm x 15 mm (0.6 in. x 0.6 in.) square.

Note: Unflowed or “dry” Honeywell PCM45 F has a material thickness of 0.010 inch. The flowed or “wet” Honeywell PCM45F has a material thickness of ~0.003 inch after it reaches its phase change temperature.

6.5.4.1 Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the bond line thickness (BLT). BLT is the final settled thickness of the thermal interface material after installation of heatsink. The effect of pressure on the thermal resistance of the Honeywell PCM45 F TIM is shown in [Table 6-3](#).

Intel provides both End of Line and End of Life TIM thermal resistance values of Honeywell PCM45F. The End of Line value represents the TIM performance post heatsink assembly while the End of Life value is the predicted TIM performance when the product and TIM reaches the end of its life. The heatsink clip provides enough pressure for the TIM to achieve End of Line thermal resistance of $0.19^{\circ}\text{C cm}^2/\text{W}$ and End of Life thermal resistance of $0.39^{\circ}\text{C cm}^2/\text{W}$.

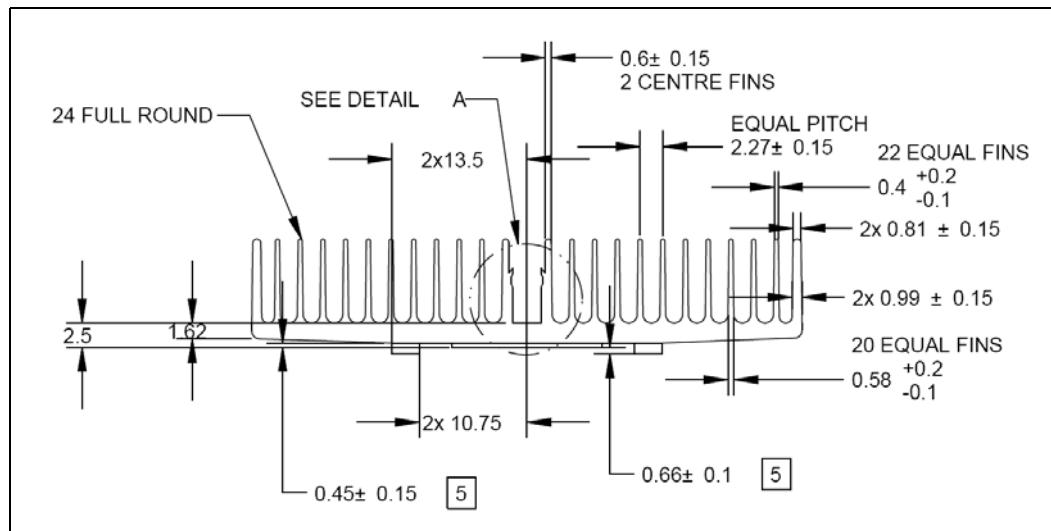
Table 6-3. Honeywell PCM45 F* TIM Performance as a Function of Attach Pressure

Pressure on Thermal solution and package interface (PSI)	Thermal Resistance ($^{\circ}\text{C} \times \text{cm}^2/\text{W}$)	
	End of Line	End of Life
40	0.19	0.39

6.5.5 Heatsink Clip

The reference solution uses a wire clip with hooked ends. The hooks attach to wire anchors to fasten the clip to the board. See [Appendix B](#) for a mechanical drawing of the clip.

Figure 6-6. Torsional Clip Heatsink Extrusion Profile



6.5.6 Clip Retention Anchors

For Intel® C600 Series Chipset-based platforms that have very limited board space, a clip retention anchor has been developed to minimize the impact of clip retention on the board. It is based on a standard three-pin jumper and is soldered to the board like any common through-hole header. A new anchor design is available with 45° bent leads to increase the anchor attach reliability over time. See [Appendix A](#) for part number and supplier information.



6.6 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume.

The test profiles for Intel® C600 Series Chipset reference solutions are unpackaged system level limits. The reference solution is to be mounted to a fully configured system. The environmental reliability requirements for the reference thermal solution are shown in [Table 6-4](#). These could be considered as general guidelines.

Table 6-4. Reliability Guidelines

Test ⁽¹⁾	Example of Test Description	Pass/Fail Criteria ⁽²⁾
Mechanical Shock	System level unpackaged test: 2 drops for + and - directions in each of 3 perpendicular axes (i.e., total 12 drops). Profile: 25g, Trapezoidal waveform, velocity change depending on system weight.	Visual Check and Electrical Functional Test
Random Vibration	System level unpackaged test: Duration: 10 min/axis, 3 axes Frequency Range: 0.002 g ² /Hz@5Hz, ramping to 0.01 g ² /Hz @20 Hz, 0.01 g ² /Hz @ 20 Hz to 500 Hz Power Spectral Density (PSD) Profile: 2.20g RMS	Visual Check and Electrical Functional Test
Temperature Cycle	-40°C to +85°C	Visual Check and Electrical Functional Test

Notes:

1. It is recommended that the above tests be performed on a sample size of at least twelve assemblies from three lots of material.
2. Additional pass/fail criteria may be added at the discretion of the user.

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Reference Thermal Solution



7

Design Recommendations for Solder Joint Reliability

Solder Joint Reliability (SJR) remains a major topic of concern in designing systems especially for surface mounted components. Solder ball cracking and fracture is a failure mode associated with overstressing the surface mounted component on the motherboard. The over-stressing typically occurs when the motherboard is subjected to bending deflection. The deflection of the motherboard applies loads to these surface mounted components that attempt to peel the component from the board. These loads stress the solder balls of the component and either initiate cracks, which grow through the solder during thermal and power cycling, or cause fracture, which results in an electrical open.

Loading conditions such as shock typically stress the motherboard and generate stresses at the solder joints that leads to either crack initiation or complete fracture of the balls. This section will discuss guidance specific to the PCH. Please refer to the *System Mechanical Design Guidance for Dynamic Events Application Note, Supporting Desktop, Workstation and Servers* for more information on system design guidance, and best practices.

[Section 2.2.2](#) describes the function of the Non-Critical to Function (NCTF) Solder Balls. These balls are located in the corners of the ball grid array, where they are most susceptible to stressing from motherboard flexure, and under the die shadow. These NCTF balls mitigate degradation to component performance once damage has occurred at the solder balls. Monitoring of these NCTF balls during shock testing is described in the Platform Design Guide. General design guidance is available in the *Desktop, Workstation, and Server System Mechanical Design Guidance for Dynamic Events*. The NCTF solder balls provide for load shedding during solder ball loading events.

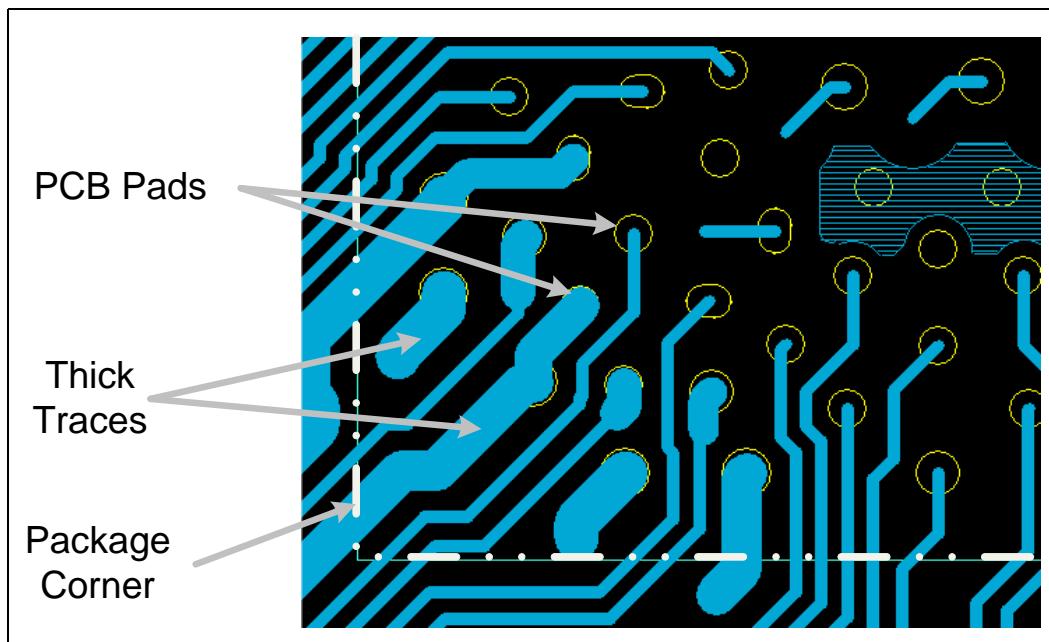
7.1

Solder Pad Recommendation

Additional protection from pad cratering on the motherboard has been demonstrated through the usage of thick traces at the corner NCTF ball locations. NCTF trace thicknesses of 60-80% of the pad diameter were tested in board level shock tests with metal define pads and reduced the occurrence of pad cratering failures. Pad cratering is the failure mode in which solder pads in the motherboard separate from the PCB.

The thick traces shown in [Figure 7-1](#) are an example of how thick traces may be used at NCTF pads. Note the NCTF locations shown in [Figure 7-1](#) are not the NCTF locations of the PCH package and is shown to illustrate the application of thick traces. Designers are encouraged to use thick traces in designs where pad cratering has occurred along the corners of the package. The thick traces effectively increase the strength of the pad to motherboard interface and may cause a crack to initiate in a different failure mode in the NCTF solder ball while increasing the shock margin.

Figure 7-1. Example of Thick Traces used in a Desktop BGA



7.2

Shock Strain Guidance

A useful metric to compare the impact of design modifications to SJR and assess SJR risk during shock events is strain measurement. This strain measurement, also referred to as shock strain, utilizes strain gages to measure the surface strain of a motherboard. Please note that Intel also publishes strain guidance specifically for manufacturing. This manufacturing guidance is part of the Board Flexure Initiative (BFI) and those strain limits are commonly referred to as BFI strain. More information is available in the BFI Manufacturing Advantage Service (MAS). **DO NOT use BFI strain values for shock strain testing and DO NOT use shock strain guidance for BFI.** These two strain metrics are significantly different and are not interchangeable. Using the BFI strain values for a design metric will likely result in a poor system design.

Given parameters unique to the board of interest, such as board thickness, the board surface strain directly correlates to the amount of board curvature. The amount of motherboard curvature in the critical locations directly beneath the solder balls is indicative of the reliability of the component solder joints. This measurement is typically made at the corners of the BGA components. The shock strain results are sensitive to the application of the strain gages. Guidance for strain gage application is available in the *Shock Strain Monitoring Customer Reference Document (CRD)*. Your Intel Corporate Quality Engineer is also available for help with strain gage attach training. This Shock Strain Monitoring CRD outlines the proper selection, application, and usage of the strain gages and strain instrumentation to attain repeatable and valid results. The Shock Strain Monitoring CRD also discusses proper reduction of the data in order to use the data to compare to the Intel strain guidance.

The strain guidance was developed from simulations and empirical testing using the Intel reference thermal solution for the PCH and Intel recommended pad types and sizes. Three strain ranges are determined to quantify associated SJR risk for the Critical



to Function solder joints. The Non-Critical to Function solder balls may have some cracking and fractures when the strain measurements are within this guidance.

Table 7-1 lists the three ranges for the PCH.

Table 7-1. Shock Strain Guidance

For 0.062" boards Shock Strain (micro strain, $\mu\epsilon$)	For 0.093" boards Shock Strain (micro strain, $\mu\epsilon$)	For 0.13" boards Shock Strain (micro strain, $\mu\epsilon$)	Associated Risk	Recommendation / Comments
Emin < 1800	Emin < 1600	Emin < 1300	Low	Solder joint failure is unlikely
1800 < Emin < 2500	1600 < Emin < 2200	1300 < Emin < 1800	Medium	Larger sample size and failure analysis is suggested for design validation
2500 < Emin	2200 < Emin	1800 < Emin	High	Solder joint failure is likely, consider design changes to improve reliability

Notes:

1. Emin is the minimum principal strain as defined in the Shock Strain Monitoring Customer Reference Document.
2. These values are for 0.062, 0.093 and 0.13 inch nominal board thickness using the solder pad definitions defined in the Customer Reference Board.
3. The strain value guidance will be different for different board thicknesses. Please contact your Intel Field Sales representative if your design uses a different board thickness.
4. These values apply to both FR4 and Halogenated Flame Retardant Free (HFR-Free) boards. See Section 7.2.1 below for more information on HFR-Free boards.

The associated risk levels correspond to the likelihood of solder joint failure. A Low level of risk is unlikely to result in critical to function solder joint failures. When strain measurements are made from a small sample of boards or systems and fall within the Medium risk range, there is insufficient information to assess the risk. It is suggested that additional systems or boards are tested and failure analysis, such as dye and peel, is conducted to assess the risk. A High risk is likely to result in a significant quantity of solder joint failures of critical solder balls. A change to the design is strongly recommended to reduce the bending of the motherboard under shock. Incorporating the Intel Reference Design Heatsink described in Chapter 6 into the design or adopting the design practices outlined in the *Desktop, Workstation, and Server System Mechanical Design Guidance for Dynamic Events* will improve the strain response and therefore reduce SJR risk.

7.2.1 Halogenated Flame Retardant Free PCB

A limited number of FR4 & Halogenated Flame Retardant Free (HFR-Free) boards available from PCB vendors were tested by Intel for shock performance and bending stiffness. Both board materials exhibited similar shock performance as measured by solder crack assessment from the dye and pull failure analysis when the optimized pad definitions were used and the mean flexural modulus of the boards were similar. The flexural modulus variations within the HFR-Free samples were significantly larger than the modulus variation observed within the FR4 samples, indicating there may be more variation in HFR-Free shock performance.

A high sensitivity to pad definition was found from the Intel testing. The usage of wide or thick traces as incorporated into the PCH pad definition was found to improve shock performance. The pad definitions defined in the Customer Reference Board are therefore **strongly recommended** for use in both HFR-Free and FR4 boards to optimize shock performance.





A Thermal Solution Component Suppliers

A.1 Torsional Clip Heatsink Thermal Solution

Table A-1. Reference Heatsink Enabled Components

Item	Intel PN	CCI	Foxconn
Heatsink Assembly • Thermal Interface Material • Torsional Clip • Insulators	E41942-003	00Z84830101	N/A
Solder-Down Anchor	A13494-008	N/A	HB9703E-DW (0.062" thick motherboard) HB9703E-M3W (0.085" thick motherboard)

Notes:

1. The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.
2. Anchor is independent of heatsink assembly. Proper Anchor selection will protect the chipset heatsink from shock and vibration.

A.2 Supplier Contact Information

Table A-2. Supplier Contact Information

Vendor Name	Contact	Phone	Email
CCI	Monica Chih	866-2-29952666, x1131(Taiwan)	monica_chih@ccic.com.tw
Foxconn	Jeff Pan Eric Ling	(909) 978-6476, (USA) (503) 693-3509, ext 225 (USA)	jeff.pan@foxconn.com eric.ling@foxconn.com

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Thermal Solution Component Suppliers



B Mechanical Drawings

Table B-1 lists the mechanical and Package drawings included in this appendix.

Table B-1. Mechanical Drawing List

Drawing Description	Figure Number
Torsional Clip Heatsink Assembly Drawing	Figure B-1
Torsional Heatsink Drawing	Figure B-2
Torsional Clip Heatsink Clip Drawing	Figure B-3
Intel C600 Series Chipset PCH Package Drawing	Figure B-4

Figure B-1. Torsional Clip Heatsink Assembly Drawing

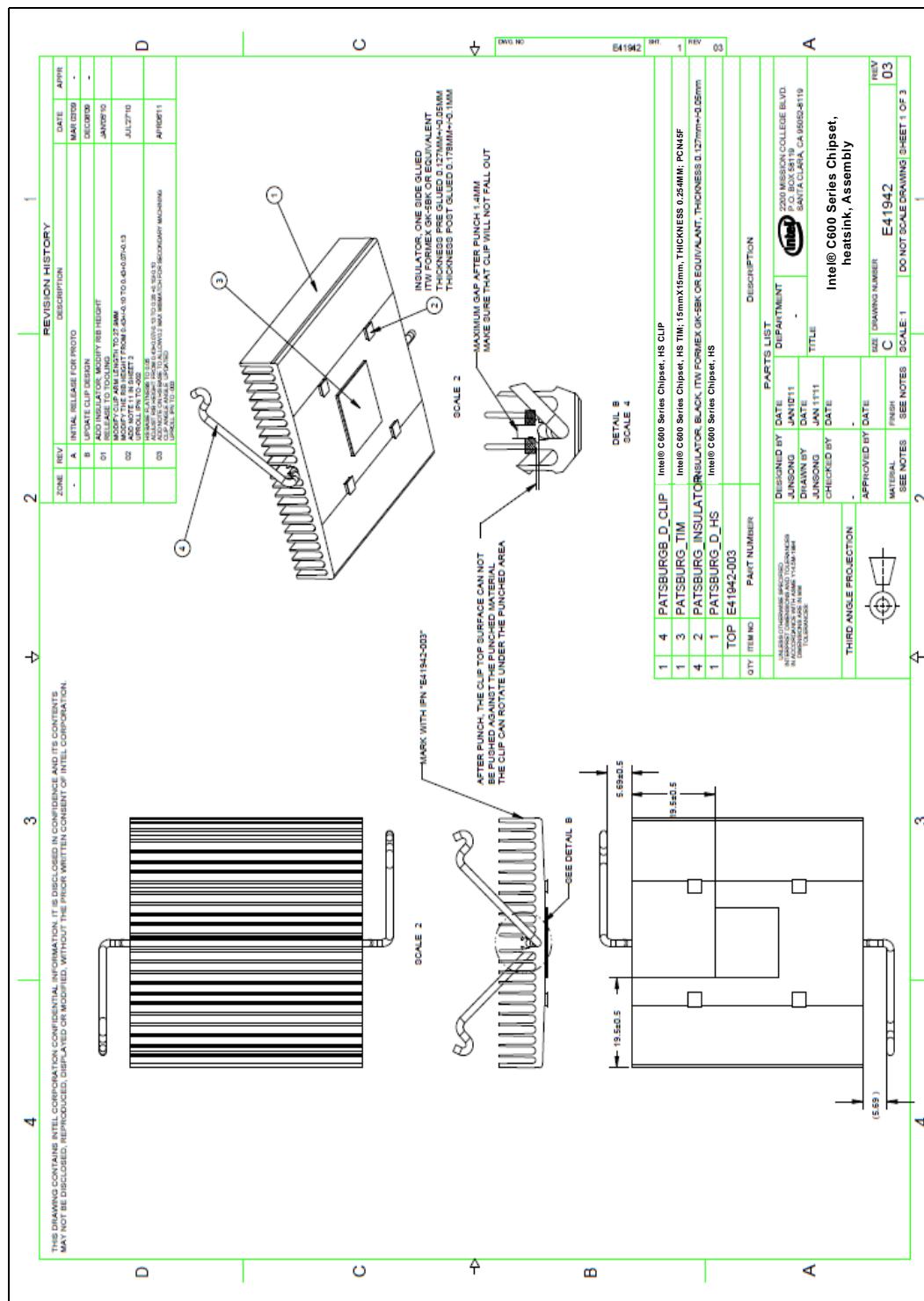




Figure B-2. Torsional Heatsink Drawing

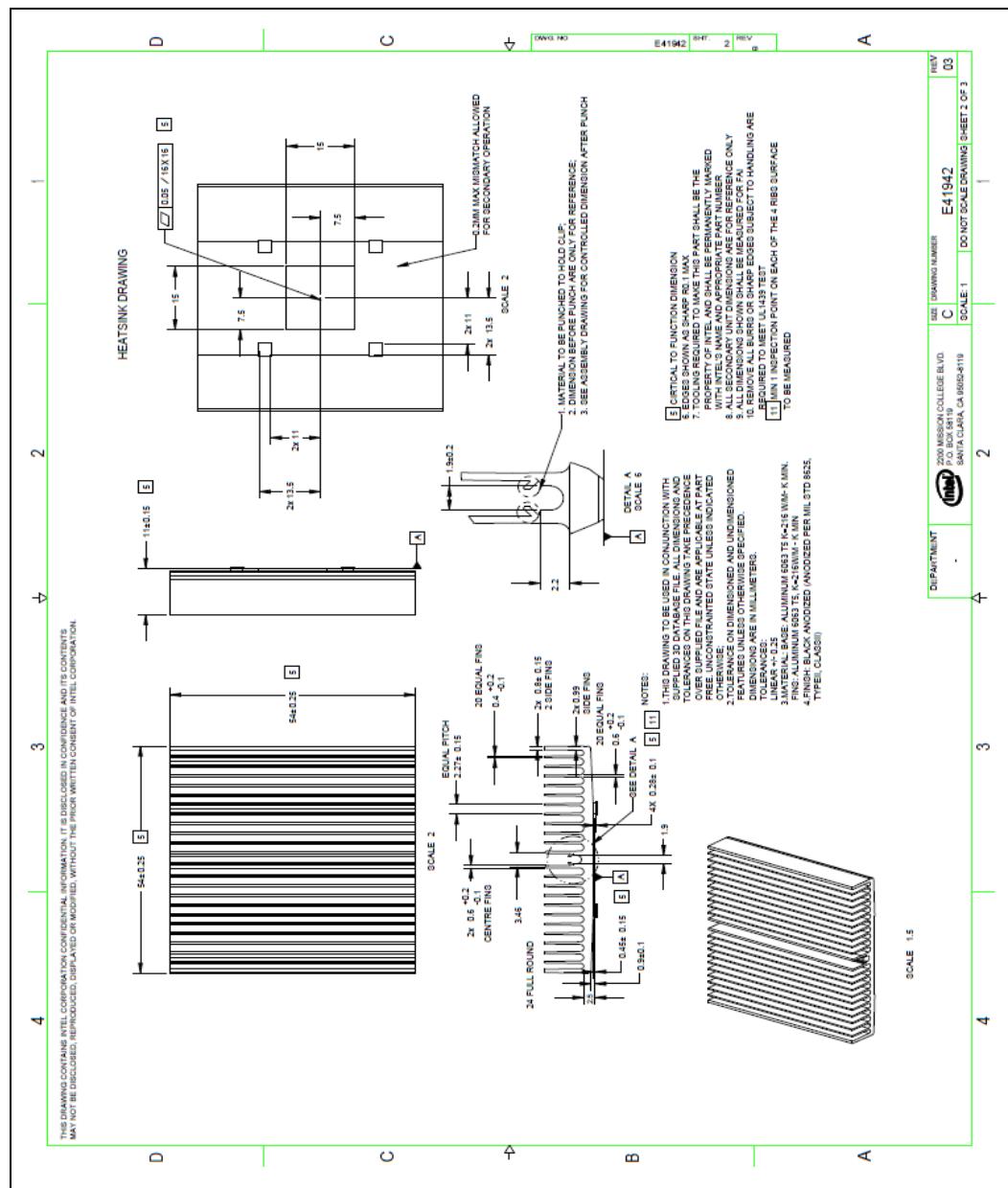


Figure B-3. Torsional Clip Heatsink Clip Drawing

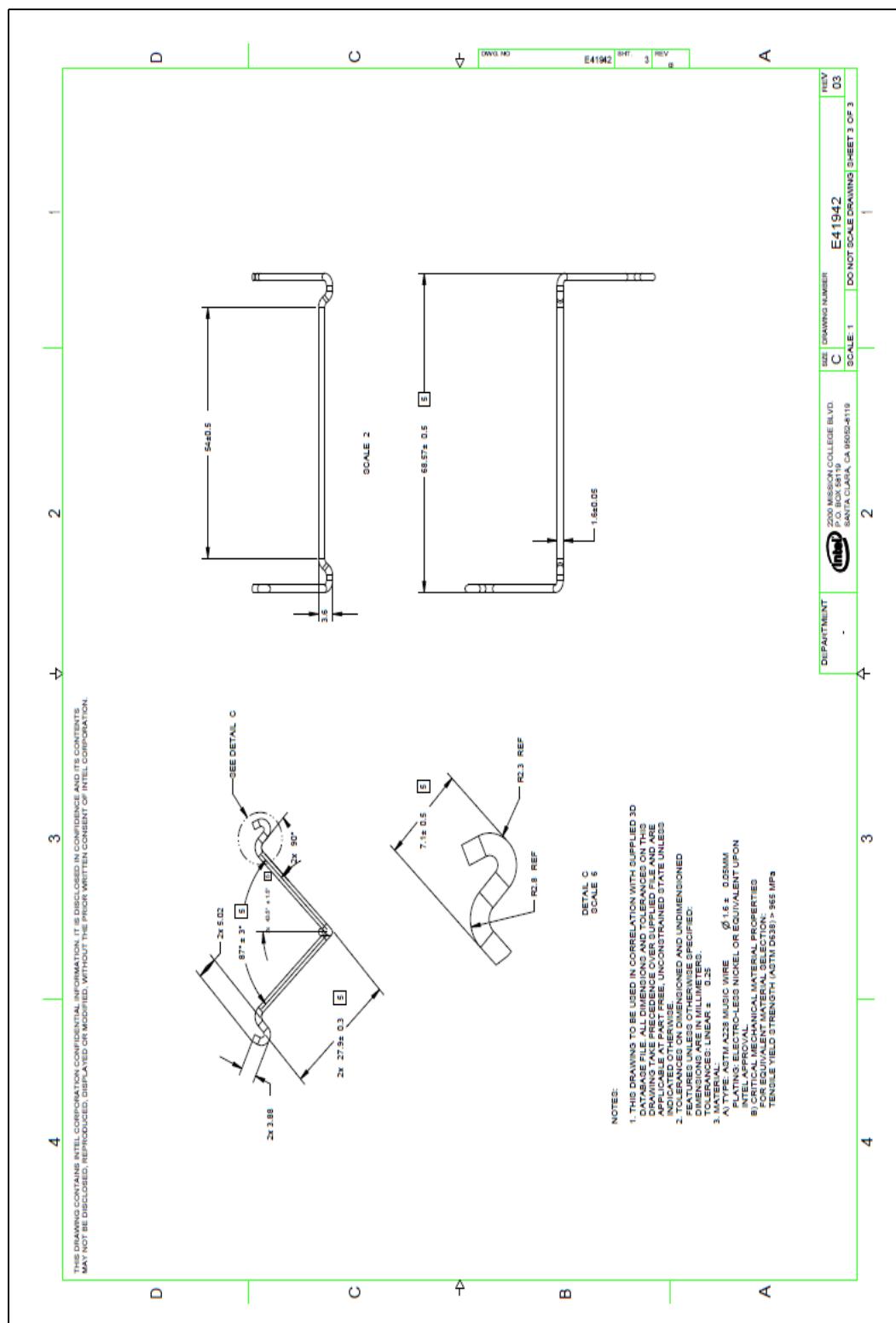
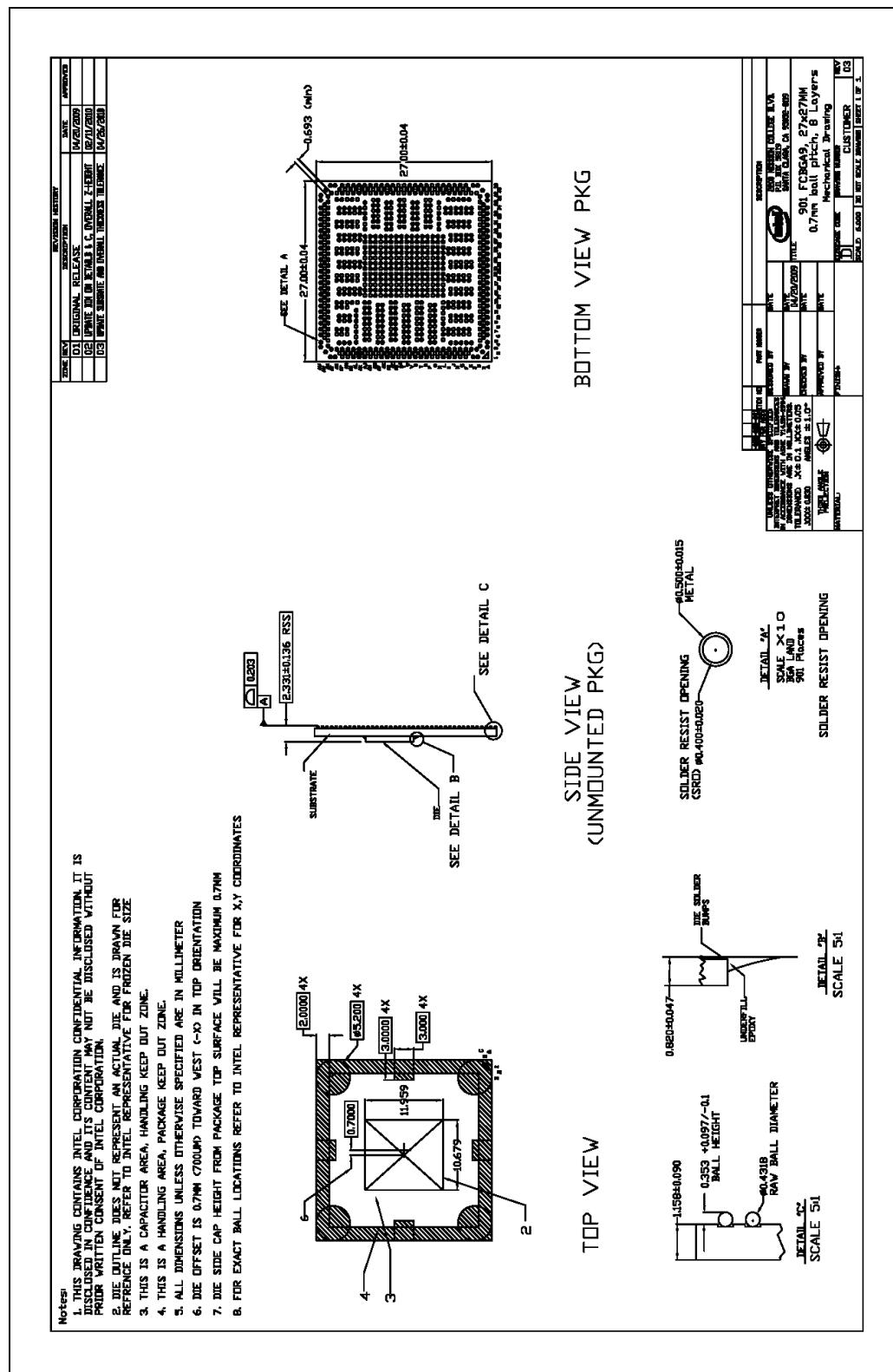




Figure B-4. Intel C600 Series Chipset PCH Package Drawing





Mechanical Drawings